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⬙ Marcelo Cintra, Diego R. Llanos
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With speculative parallelization, code sections that cannot be fully analy
executed in parallel. Hardware schemes are fast but expensive and requ
memory system. Software schemes ...

Keywords: speculative parallelization, thread-level speculation

Also published in:
   October 2003 **SIGPLAN Notices** Volume 38 Issue 10

2 Transient fault prediction based on anomalies in processor events
Satish Narayanasamy, Ayse K. Coskun, Brad Calder
April 2007   **DATE '07:** Proceedings of the conference on Design, automa
Publisher: EDA Consortium
Full text available: ▤Pdf (173.56 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 26, Downloa

Future microprocessors will be highly susceptible to transient errors as 1
scaling. Prior techniques advocated full scale structural or temporal redu
they can provide ...

3 Exploiting reference idempotency to reduce speculative storage ove⎺
⬙ Seon Wook Kim, Chong-Liang Ooi, Rudolf Eigenmann, Babak Falsafi, T. N.
September 2006 **Transactions on Programming Languages and Syster**
Publisher: ACM ⦿ Request Permissions
Full text available: ▤Pdf (433.96 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 33, Downloa

Recent proposals for multithreaded architectures employ speculative ex
dependences to execute speculatively in parallel. The architectures use

speculative data, track data dependences ...

Keywords: Idempotent references, compiler-assisted speculative execu

4   Recovery code generation for general speculative optimizations
Jin Lin, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin-Fook Ngai
March 2006   **Transactions on Architecture and Code Optimization (T**
Publisher: ACM Request Permissions
Full text available: Pdf (909.58 KB)   Additional Information: full citation, absf

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 45, Downloa

A general framework that integrates both control and data speculation t
rules has shown to improve CPU2000 performance on Itanium systems.
check instructions and ...

Keywords: Recovery code, multi-level data speculation, speculative SS

5   A Compiler Framework for Recovery Code Generation in General Sp
Jin Lin, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin-Fook Ngai
September 2004 **PACT '04:** Proceedings of the 13th International Conferen
                     Techniques
Publisher: IEEE Computer Society
Full text available: Pdf (186.86 KB)   Additional Information: full citation, absf

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 17, Downloa

A general framework that integrates both control and data speculation t
rules has shown to improve SPEC2000 performance on Itanium systems
check instructions and ...

6   Simultaneous speculative threading: a novel pipeline architecture im
Shailender Chaudhry, Robert Cypher, Magnus Ekman, Martin Karlsson, Anc
Tremblay
June 2009   **ISCA '09:** Proceedings of the 36th annual international symp
Publisher: ACM Request Permissions
Full text available: Pdf (1.30 MB)   Additional Information: full citation, absf

Bibliometrics: Downloads (6 Weeks): 53, Downloads (12 Months): 749, Downl

This paper presents Simultaneous Speculative Threading (SST), which i:
area- and power-efficient cores for chip multiprocessors. SST hardware
from a single sequential ...

Keywords: checkpoint-based architecture, chip multiprocessor, cmp, h
parallelism, memory-level parallelism, processor architecture, sst

Also published in:
   June 2009 **SIGARCH Computer Architecture News** Volume 37 Issue 3

7   CAVA: Using checkpoint-assisted value prediction to hide L2 misses

Luis Ceze, Karin Strauss, James Tuck, Josep Torrellas, Jose Renau
June 2006   **Transactions on Architecture and Code Optimization (T.**
Publisher: ACM ✧ Request Permissions
Full text available: 📄 Pdf (646.62 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 44, Downloa

Modern superscalar processors often suffer long stalls because of load n
problem, we propose hiding L2 misses with Checkpoint-Assisted VAlue p
predicted value is returned …

Keywords: Value prediction, checkpointed processor architectures, me

8 A model to exploit power-performance efficiency in superscalar proc
Omer Khan, Sandip Kundu
May 2010   **GLSVLSI '10:** Proceedings of the 20th symposium on Great I
Publisher: ACM ✧ Request Permissions
Full text available: 📄 Pdf (770.85 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 7, Download

Power consumption has become a major cause of concern spanning fror
Traditionally, improvement in power-performance efficiency of a moderi
scaling. However, that is no longer …
Keywords: modeling, power

9 Incrementally parallelizing database transactions with thread-level sp
Christopher B. Colohan, Anastassia Ailamaki, J. Gregory Steffan, Todd C. M
February 2008 **Transactions on Computer Systems (TOCS)** , Volume 26 Is
Publisher: ACM ✧ Request Permissions
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Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 159, Downlo

With the advent of chip multiprocessors, exploiting intratransaction par
way of improving transaction performance. However, exploiting intratra
reasons: first, significant …

Keywords: Thread-level speculation, chip-multiprocessing, incrementa

10 Pinot: Speculative Multi-threading Processor Architecture Exploiting
Granularities
Taku Ohsawa, Masamichi Takagi, Shoji Kawahara, Satoshi Matsushita
November 2005 **MICRO 38:** Proceedings of the 38th annual IEEE/ACM Inte
Publisher: IEEE Computer Society
Full text available: 📄 Publisher Site , 📄 Pdf (592.97 KB) Additional Information: full citatio

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 48, Downloa

We propose a speculative multi-threading processor architecture called
range of granularities without modifying program sources. Since exploit
limits of parallelism …

11 Structure-driven optimizations for amorphous data-parallel programs

Mario Méndez-Lojo, Donald Nguyen, Dimitrios Prountzos, Xin Sui, M. Ambe Keshav Pingali

January 2010 **PPoPP '10:** Proceedings of the 15th ACM SIGPLAN symposiu programming

Publisher: ACM Request Permissions

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Bibliometrics: Downloads (6 Weeks): 37,   Downloads (12 Months): 154,   Downl

Irregular algorithms are organized around pointer-based data structure: ubiquitous in applications. Recent work by the Galois project has provid irregular applications based ...

Keywords: amorphous data-parallelism, cautious operator implementa coalescing, one-shot optimization, optimistic parallelization, synchroniza

12 POSH: a TLS compiler that exploits program structure

Wei Liu, James Tuck, Luis Ceze, Wonsun Ahn, Karin Strauss, Jose Renau, J

March 2006   **PPoPP '06:** Proceedings of the eleventh ACM SIGPLAN symp programming

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Bibliometrics: Downloads (6 Weeks): 8,   Downloads (12 Months): 66,   Downloa

As multi-core architectures with Thread-Level Speculation (TLS) are bec focus on TLS compilation. TLS compilers are interesting in that, while th independence of concurrent tasks, ...

Keywords: TLS compiler, multi-core architecture, prefetching, profiling

13 A probabilistic pointer analysis for speculative optimizations

Jeff Da Silva, J. Gregory Steffan

November 2006 **ASPLOS-XII:** Proceedings of the 12th international confere programming languages and operating systems

Publisher: ACM Request Permissions

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Bibliometrics: Downloads (6 Weeks): 14,   Downloads (12 Months): 79,   Downlo

Pointer analysis is a critical compiler analysis used to disambiguate the the use of pointers and pointer-based data structures. A conventional p pointers, at any program ...

Keywords: dependence analysis, pointer analysis, speculative optimiza

Also published in:

October 2006   **SIGARCH Computer Architecture News** Volume 34 Issue 5
October 2006   **SIGOPS Operating Systems Review**   Volume 40 Issue 5

14 Decoupled Software Pipelining with the Synchronization Array
Ram Rangan, Neil Vachharajani, Manish Vachharajani, David I. August
September 2004 **PACT '04:** Proceedings of the 13th International Conferen
        Techniques
Publisher: IEEE Computer Society
Full text available: Pdf (311.44 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 5,   Downloads (12 Months): 62,   Downloa

Despite the success of instruction-level parallelism (ILP) optimizations ii
microprocessors, certain codes remain elusive. In particular, codes cont
traversal loops have been largely ...

15 On approximating the ideal random access machine by physical mac
Gianfranco Bilardi, Kattamuri Ekanadham, Pratap Pattnaik
August 2009 **Journal of the ACM (JACM)** , Volume 56 Issue 5
Publisher: ACM Request Permissions
Full text available: Pdf (834.87 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 11,   Downloads (12 Months): 223,   Downl

The capability of the *Random Access Machine* (RAM) to execute any insl
to fundamental physical constraints on the minimum size of devices anc
explores how ...

Keywords: Physical constraints on machines, pipelined hierarchical me

16 ReSlice: Selective Re-Execution of Long-Retired Misspeculated Insti
Smruti R. Sarangi, Wei Liu, Josep Torrellas, Yuanyuan Zhou
November 2005 **MICRO 38:** Proceedings of the 38th annual IEEE/ACM Inte
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (428.43 KB) Additional Information: full citatio

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As more data value speculation mechanisms are being proposed to spee
on the critical processor structures that must buffer the state of the spe
checkpoint the processor ...

17 Inferential queueing and speculative push for reducing critical comm
Ravi Rajwar, Alain Kägi, James R. Goodman
June 2003   **ICS '03:** Proceedings of the 17th annual international confere
Publisher: ACM Request Permissions
Full text available: Pdf (568.93 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 0,   Downloads (12 Months): 26,   Downloa

Communication latencies within critical sections constitute a major bottl
workloads. In this paper, we argue for the use of Inferentially Queued L
synchronization but also ...

Keywords: data forwarding, inferential queueing, synchronization

18 Extending concurrency of transactional memory programs by using \
Salil Mohan Pant, Gregory T. Byrd
May 2009   **CF '09**: Proceedings of the 6th ACM conference on Computing
Publisher: ACM ◇ Request Permissions
Full text available: Pdf (877.06 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 118, Downlo

Transactional Memory (TM) is an optimistic speculative synchronization
region of code marked as a transaction by the programmer. TM avoids i
based synchronization and ...

Keywords: logtm, transactional memory, value prediction

19 An integrated hardware-software approach to flexible transactional n
Arrvindh Shriraman, Michael F. Spear, Hemayet Hossain, Virendra J. Marat
June 2007   **ISCA '07**: Proceedings of the 34th annual international symp
Publisher: ACM ◇ Request Permissions
Full text available: Pdf (637.98 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 21, Downloads (12 Months): 147, Downl

There has been considerable recent interest in both hardware andsoftwa
an intermediateapproach, in which hardware serves to accelerate a TM i
software. Specifically, we ...

Keywords: RSTM, cache coherence, multiprocessors, transactional mei

Also published in:
June 2007 **SIGARCH Computer Architecture News** Volume 35 Issue 2

20 Fire-and-Forget: Load/Store Scheduling with No Store Queue at All
Samantika Subramaniam, Gabriel H. Loh
December 2006 **MICRO 39**: Proceedings of the 39th Annual IEEE/ACM Inte
Publisher: IEEE Computer Society
Full text available: Pdf (357.14 KB)   Additional Information: full citation, abst

Bibliometrics: Downloads (6 Weeks): 9, Downloads (12 Months): 68, Downloa

Modern processors use CAM-based load and store queues (LQ/SQ) to su
store-to-load forwarding. However, the LQ and SQ scale poorly for the s
processors. Past research has ...

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   With speculative parallelization, code sections that cannot be fully analy
   parallel. Hardware schemes are fast but expensive and require modifica
   Software schemes ...

   Keywords: speculative parallelization, thread-level speculation

   Also published in:
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2 Inferential queueing and speculative push for reducing critical comm
   Ravi Rajwar, Alain Kägi, James R. Goodman
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   Communication latencies within critical sections constitute a major bottl
   workloads. In this paper, we argue for the use of Inferentially Queued L
   synchronization but also ...

   Keywords: data forwarding, inferential queueing, synchronization

3 Exploiting multiple functionality for nano-scale reconfigurable system
   Paul Beckett
   April 2003   **GLSVLSI '03:** Proceedings of the 13th ACM Great Lakes sym
   Publisher: ACM 🔧 Request Permissions

Bibliometrics: Downloads (6 Weeks): 7,   Downloads (12 Months): 41,   Downloa

It is likely that it will become increasingly difficult to manufacture the co
characterise current reconfigurable logic systems. As a result, these sys
of largely ...

Keywords: RTD, carbon nanotube, chalcogenide, double gate transisto
nanoelectronics, nanotechnology, reconfigurable systems, resonant tun

4 Load and store reuse using register file contents
Soner Önder, Rajiv Gupta
June 2001   **ICS '01:** Proceedings of the 15th international conference on
Publisher: ACM Request Permissions
Full text available: Pdf (251.51 KB)   Additional Information: full citation, at

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The detection of opportunities for value reuse optimizations in memory
associated with these operations to be available. Although the values ar
their ...

5 Reference idempotency analysis: a framework for optimizing specula
Seon Wook Kim, Chong-liang Ooi, Rudolf Eigenmann, Babak Falsafi, T. N. \
July 2001   **PPoPP '01:** Proceedings of the eighth ACM SIGPLAN sympos
programming
Publisher: ACM Request Permissions
Full text available: Pdf (329.79 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 3,   Downloads (12 Months): 20,   Downloa

Recent proposals for multithreaded architectures allow threads with unk
parallel. These architectures use hardware speculative storage to buffer
roll ...

Also published in:
July 2001 **SIGPLAN Notices** Volume 36 Issue 7

6 A general compiler framework for speculative multithreading
Anasua Bhowmik, Manoj Franklin
August 2002   **SPAA '02:** Proceedings of the fourteenth annual ACM sympo
Publisher: ACM Request Permissions
Full text available: Pdf (231.41 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 5,   Downloads (12 Months): 90,   Downloa

Speculative multithreading (SpMT) promises to be an effective mechani
tend to use irregular data structures with pointers and have complex flo
obtaining ...

Keywords: TLP compiler, control dependence, data dependence, parall

thread formation, thread-level parallelism (TLP)

7 Register Synthesis for Speculative Computation
Dirk Herrmann, Rolf Ernst
March 1997   **EDTC '97:** Proceedings of the 1997 European conference on
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (639.76 KB) Additional Information: full citatio

Bibliometrics: Downloads (6 Weeks): 0,   Downloads (12 Months): 1,   Download

Speculative computation and branch prediction have been used in high-
Recently, it has also been applied to high-level synthesis where a priori
even higher performance ...

Keywords: high-level-synthesis, register synthesis, life time analysis, ‹

8 Containers on the Parallelization of General-Purpose Java Programs
Peng Wu, David Padua
October 1999 **PACT '99:** Proceedings of the 1999 International Conference
Techniques
Publisher: IEEE Computer Society
Full text available: Publisher Site   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): n/a,   Downloads (12 Months): n/a,   Downl

Automatic parallelization of general-purpose programs is still not possib
structures and complex control-flows. One promising strategy is tread-l‹
alleviates the ...

Keywords: compiler parallelization, dependence test, Java parallelizatic

9 Parallel multiplication: a case study in parallel programming
C. K. Yuen, M. D. Feng
March 1994   **SIGPLAN Notices** , Volume 29 Issue 3
Publisher: ACM
Full text available: Pdf (437.48 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 2,   Downloads (12 Months): 29,   Downloa

Six versions of a parallel program for multiplication are presented, and ‹
illustrate the bottom up and top down methods of program structure de
processing in ...

10 Performance modelling of speculative prefetching for compound requ
N. J. Tuah, M. J. Kumar, S. Venkatesh
August 2000   **WOWMOM '00:** Proceedings of the 3rd ACM international wc
Publisher: ACM Request Permissions
Full text available: Pdf (817.34 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 1,   Downloads (12 Months): 8,   Download

To improve the accuracy of access prediction, a prefetcher for web brov

a compound. By this term we mean that a user request for a single web
multimedia items. ...

Keywords: Web, caching, compound requests, speculative prefetching

11 Pointer cache assisted prefetching
Jamison Collins, Suleyman Sair, Brad Calder, Dean M. Tullsen
November 2002 **MICRO 35:** Proceedings of the 35th annual ACM/IEEE inter
Publisher: IEEE Computer Society Press
Full text available: Publisher Site , Pdf (1.21 MB) Additional Information: full citation,

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 31, Downloa

Data prefetching effectively reduces the negative effects of long load lat
Hardware prefetchers employ hardware structures to predict future mer
Thread-based prefetchers ...

12 A fill-unit approach to multiple instruction issue
Manoj Franklin, Mark Smotherman
November 1994 **MICRO 27:** Proceedings of the 27th annual international sy
Publisher: ACM
Full text available: Pdf (992.94 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 19, Downloa

Multiple issue of instructions occurs in superscalar and VLIW machines.
design, which combines the advantages of code compatibility as in supe
checking logic ...

Keywords: VLIW, instruction-level parallelism, multiple operation issue

13 Streamlining inter-operation memory communication via data depend
Andreas Moshovos, Gurindar S. Sohi
December 1997 **MICRO 30:** Proceedings of the 30th annual ACM/IEEE inter
Publisher: IEEE Computer Society
Full text available: Publisher Site , Pdf (1.73 MB) Additional Information: full citation,

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 23, Downloa

We revisit memory hierarchy design viewing memory as an inter-operat
to the development of novel methods of performing inter-operation mer
prediction to identify ...

Keywords: DEF-store-load-USE chains, address calculation, address di
access, data cache bandwidth requirements, data dependence predictio
communication, memory architecture, memory dependences, memory l
value cache

14 Dynamically assembled documentation
Michael Priestley
October 1999 **SIGDOC '99:** Proceedings of the 17th annual international co

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Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 9, Download

As online information becomes more comprehensive in its scope, the sh
Information needs to be both browsable and searchable, and both need
approach (such as SGML ...

Keywords: dynamic documentation, reference documentation, structui

15 A retrospective on the Dorado, a high-performance personal comput
Kenneth A. Pier
June 1983   **ISCA '83:** Proceedings of the 10th annual international symp
Publisher: ACM
Full text available: ⌗ Pdf (2.01 MB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 30, Downloa

In late 1975, members of the Xerox Palo Alto Research Center embarke
successor to the Alto personal minicomputer, in use since 1973. After fc
Dorado, was in use within ...

Also published in:
   June 1983 **SIGARCH Computer Architecture News** Volume 11 Issue 3

16 Architectural support for scalable speculative parallelization in share
Marcelo Cintra, José F. Martínez, Josep Torrellas
June 2000   **ISCA '00:** Proceedings of the 27th annual international symp
Publisher: ACM
Full text available: ⌗ Pdf (253.29 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 76, Downloa

Speculative parallelization aggressively executes in parallel codes that c
proposals of hardware schemes have mostly focused on single-chip mul
necessarily limited ...

Also published in:
   May 2000 **SIGARCH Computer Architecture News** Volume 28 Issue 2

17 A compiler framework for speculative analysis and optimizations
Jin Lin, Tong Chen, Wei-Chung Hsu, Pen-Chung Yew, Roy Dz-Ching Ju, Tin
June 2003   **PLDI '03:** Proceedings of the ACM SIGPLAN 2003 conference
                  implementation
Publisher: ACM ⌗ Request Permissions
Full text available: ⌗ Pdf (323.88 KB)   Additional Information: full citation, at

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Speculative execution, such as control speculation and data speculation
performance. Using edge/path profile information or simple heuristic rul
incorporate and exploit ...

Keywords: data speculation, partial redundancy elimination, register p
update

Also published in:
   May 2003 **SIGPLAN Notices** Volume 38 Issue 5

18 The Jrpm system for dynamically parallelizing Java programs
Michael K. Chen, Kunle Olukotun
June 2003   **ISCA '03:** Proceedings of the 30th annual international symp
Publisher: ACM
Full text available: Pdf (320.42 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 7,   Downloads (12 Months): 73,   Downloa

We describe the Java runtime parallelizing machine (Jrpm), a complete
automatically. Jrpm is based on a chip multiprocessor (CMP) with threac
sharing and communication ...

Also published in:
   May 2003 **SIGARCH Computer Architecture News** Volume 31 Issue 2

19 Computing curricula 2001
CORPORATE The Joint Task Force on Computing Curricula
September 2001 **Journal on Educational Resources in Computing (JER**
Publisher: ACM Request Permissions
Full text available: Html (2.78 KB), Pdf (613.63 KB) Additional Information: full citatic

Bibliometrics: Downloads (6 Weeks): 91,   Downloads (12 Months): 1091,   Dowr

20 An evaluation of speculative instruction execution on simultaneous n
Steven Swanson, Luke K. McDowell, Michael M. Swift, Susan J. Eggers, Hei
August 2003   **Transactions on Computer Systems (TOCS)** , Volume 21 Iss
Publisher: ACM Request Permissions
Full text available: Pdf (578.85 KB)   Additional Information: full citation, at

Bibliometrics: Downloads (6 Weeks): 3,   Downloads (12 Months): 44,   Downloa

Modern superscalar processors rely heavily on speculative execution for
show that on a 6-issue superscalar, 93% of committed instructio
speculation, processor ...

Keywords: Instruction-level parallelism, multiprocessors, multithreadir
thread-level parallelism

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1 Process migration
◈ Dejan S. Milojičić, Fred Douglis, Yves Paindaveine, Richard Wheeler, Songn
  September 2000 **Computing Surveys (CSUR)** , Volume 32 Issue 3
  Publisher: ACM ✦ Request Permissions
  Full text available: 📄Pdf (1.24 MB)   Additional Information: full cit

  Bibliometrics: Downloads (6 Weeks): 49, Downloads (12 Months): 611,   Downl

  Process migration is the act of transferring a process between two macl
  system administration, and data access locality. Despite these goals an

  Keywords: distributed operating systems, distributed systems, load di:

2 Principled design of the modern Web architecture
◈ Roy T. Fielding, Richard N. Taylor
  May 2002   **Transactions on Internet Technology (TOIT)** , Volume 2
  Publisher: ACM ✦ Request Permissions
  Full text available: 📄Pdf (335.47 KB)   Additional Information: full cit

  Bibliometrics: Downloads (6 Weeks): 69, Downloads (12 Months): 518,   Downl

  The World Wide Web has succeeded in large part because its software a
  distributed hypermedia application. The modern Web architecture emph

  Keywords: Network-based applications, REST, World Wide Web

3 Extended ephemeral logging: log storage management for applicatio
◈ John S. Keen, William J. Dally
  March 1997 **Transactions on Database Systems (TODS)** , Volume 22 Issue
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  Keywords: OLTP, disk management, logging, long transactions

4

The design of an acquisitional query processor for sensor networks
Samuel Madden, Michael J. Franklin, Joseph M. Hellerstein, Wei Hong
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We discuss the design of an acquisitional query processor for data collec
where, when, and how often data is physically acquired (*sampled*) and

5 Principled design of the modern Web architecture
Roy T. Fielding, Richard N. Taylor
June 2000   **ICSE '00:** Proceedings of the 22nd international conferenc
Publisher: ACM
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The World Wide Web has succeeded in large part because its software a
distributed hypermedia system. The modern Web architecture emphasiz

Keywords: WWW, software architectural style, software architecture

6 Disconnection modes for mobile databases
Joanne Holliday, Divyakant Agrawal, Amr El Abbadi
July 2002   **Wireless Networks** , Volume 8 Issue 4
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As mobility permeates into todays computing and communication arena
mobile technologies. Traditional database applications and information s

Keywords: data consistency, databases, disconnected operation, mobi

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Patrick Chiu, Lynn Wilcox
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Keywords: audio, clustering multimedia, emergent structure, freeform
marking, note-taking

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August 2001   **IEEE/ACM Transactions on Networking (TON)** , Volume
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Simulating how the global Internet behaves is an immensely challenging
change. The heterogeneity ranges from the individual links that carry th

Keywords: Internet, modeling, simulation

9 Formal verification of standards for distance vector routing protocols
Karthikeyan Bhargavan, Davor Obradovic, Carl A. Gunter
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We show how to use an interactive theorem prover, HOL, together with
routing protocols. We do three case studies: correctness of the RIP stan

Keywords: AODV, Formal verification, HOL, RIP, SPIN, distance vector
standards, routing protocols

10 A practical comparison between Java and Ada in implementing a rea
Eric Potratz
December 2003   **SigAda '03:** Proceedings of the 2003 annual ACM SIGAda
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This paper presents a student's observations from an undergraduate res
a real-time embedded system that was originally implemented in a univ

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programming, package elaboration, performance, priority inversion, rea

Also published in:
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Dan Gunter, Brian L. Tierney, Craig E. Tull, Vibha Virmani
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Typical Grid computing scenarios involve manydistributed hardware anc
more likely it is that oneof them may fail. In order for Grid computing to

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Kate Larson, Tuomas Sandholm
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An alternating offers bargaining model for computationally limited agen
restrict them from determining an optimal solution. As the agents comp

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Cluster-based servers can substantially increase performance when nod
show that cooperation results in a substantial availability loss, in the ab

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Michael Terry, Elizabeth D. Mynatt
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We introduce Side Views, a user interface mechanism that provides on-
are designed to explicitly support the practices and needs of expert use

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Interruptible rendering is a novel approach to the fidelity-versus-perforr
rendering unifies spatial error caused by rendering coarse approximatio

Keywords: level of detail, mesh simplification, perceptually motivated

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Bernhard Zeller, Alfons Kemper
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The database volumes of enterprise resource planning (ERP) systems lil
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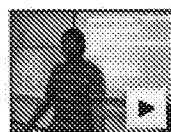
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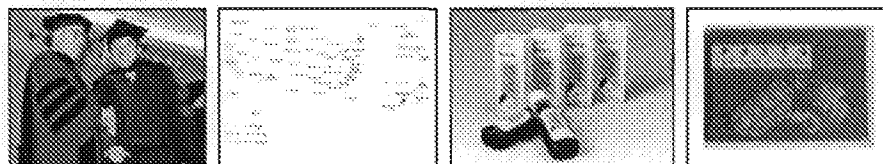
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